REG10J0131-0100

# Renesas Starter Kit for H8SX/1668R

# User's Manual

RENESAS SINGLE-CHIP MICROCOMPUTER
H8SX FAMILY

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# Chapter 1. Preface

## Cautions

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## Glossary

| | | | |
|---|---|---|---|
| CPU | Central Processing Unit | HEW | High-performance Embedded Workshop |
| LED | Light Emitting Diode | RSK | Renesas Starter Kit |
| PC | Program Counter | E10A FSK | On-chip debugger module |
| LCD | Liquid Crystal Display | DAC | Digital-to-Analog Converter |

# Chapter 2. Purpose

This RSK is an evaluation tool for Renesas microcontrollers.

This manual describes the technical details of the RSK hardware. The Quick Start Guide and Tutorial Manual provide details of the software installation and debugging environment.

Features include:

- Renesas Microcontroller Programming.
- User Code Debugging.
- User Circuitry such as Switches, LEDs and potentiometer.
- User or Example Application.
- Sample peripheral device initialisation code.

The RSK board contains all the circuitry required for microcontroller operation.

# Chapter 3. Power Supply

## 3.1. Requirements

This RSK operates from a 5V power supply.

A diode provides reverse polarity protection only if a current limiting power supply is used.

All RSK boards are supplied with an E10A debugger.

All RSK boards have an optional centre positive supply connector using a 2.0mm barrel power jack.

Warning

The RSK is neither under nor over voltage protected. Use a centre positive supply for this board.

## 3.2. Power – Up Behaviour

When the RSK is purchased the RSK board has the ‘Release’ or stand alone code from the example tutorial code pre-programmed into the Renesas microcontroller. On powering up the board the user LEDs will start to flash. After 200 flashes, or after pressing a switch the LEDs will flash at a rate controlled by the potentiometer.

# Chapter 4. Board Layout

## 4.1. Component Layout

The following diagram shows top layer component layout of the board.

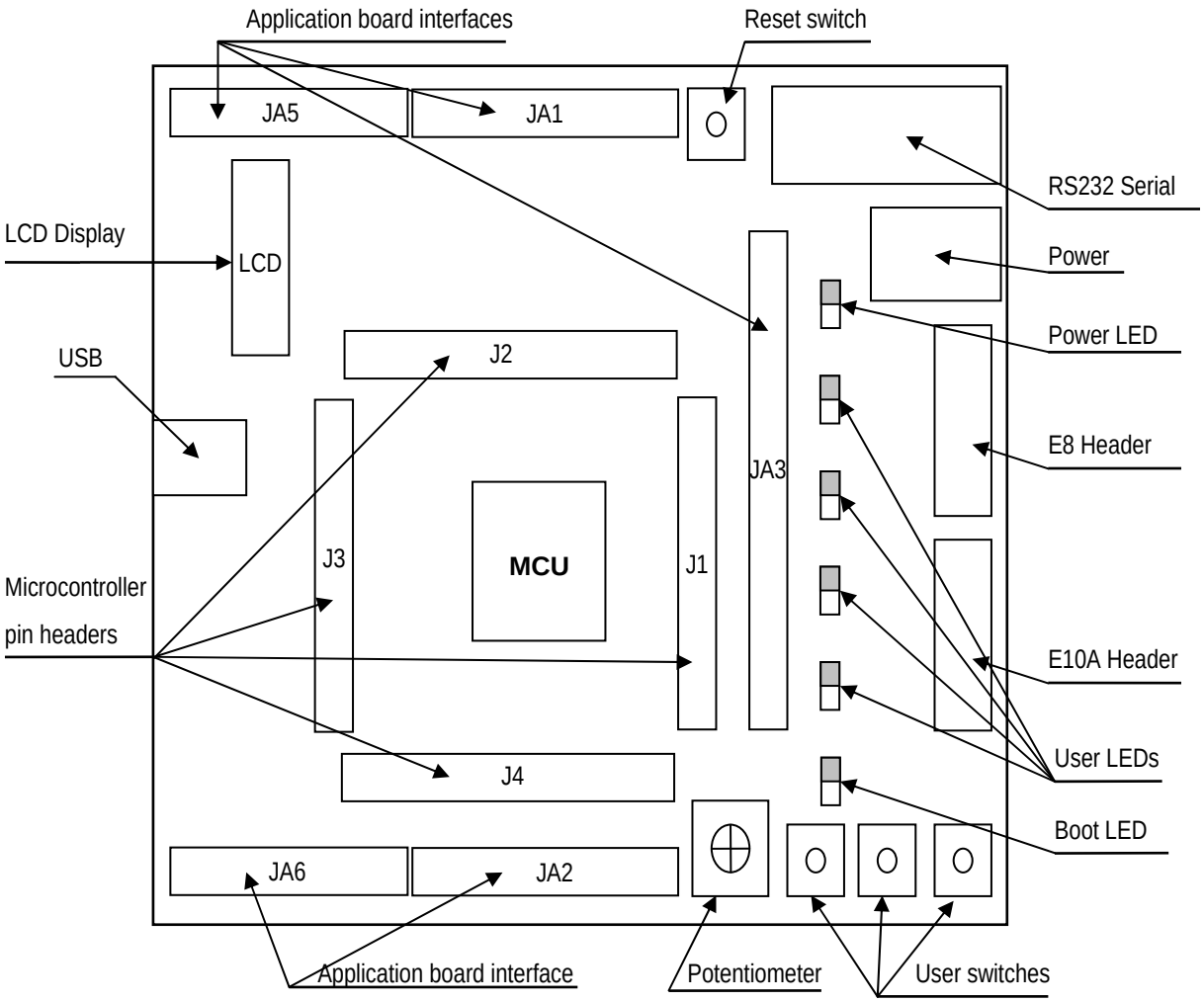



Figure 4-1: Board Layout

## 4.2. Board Dimensions

The following diagram gives the board dimensions and connector positions. All through hole connectors are on a common 0.1" grid for easy interfacing.

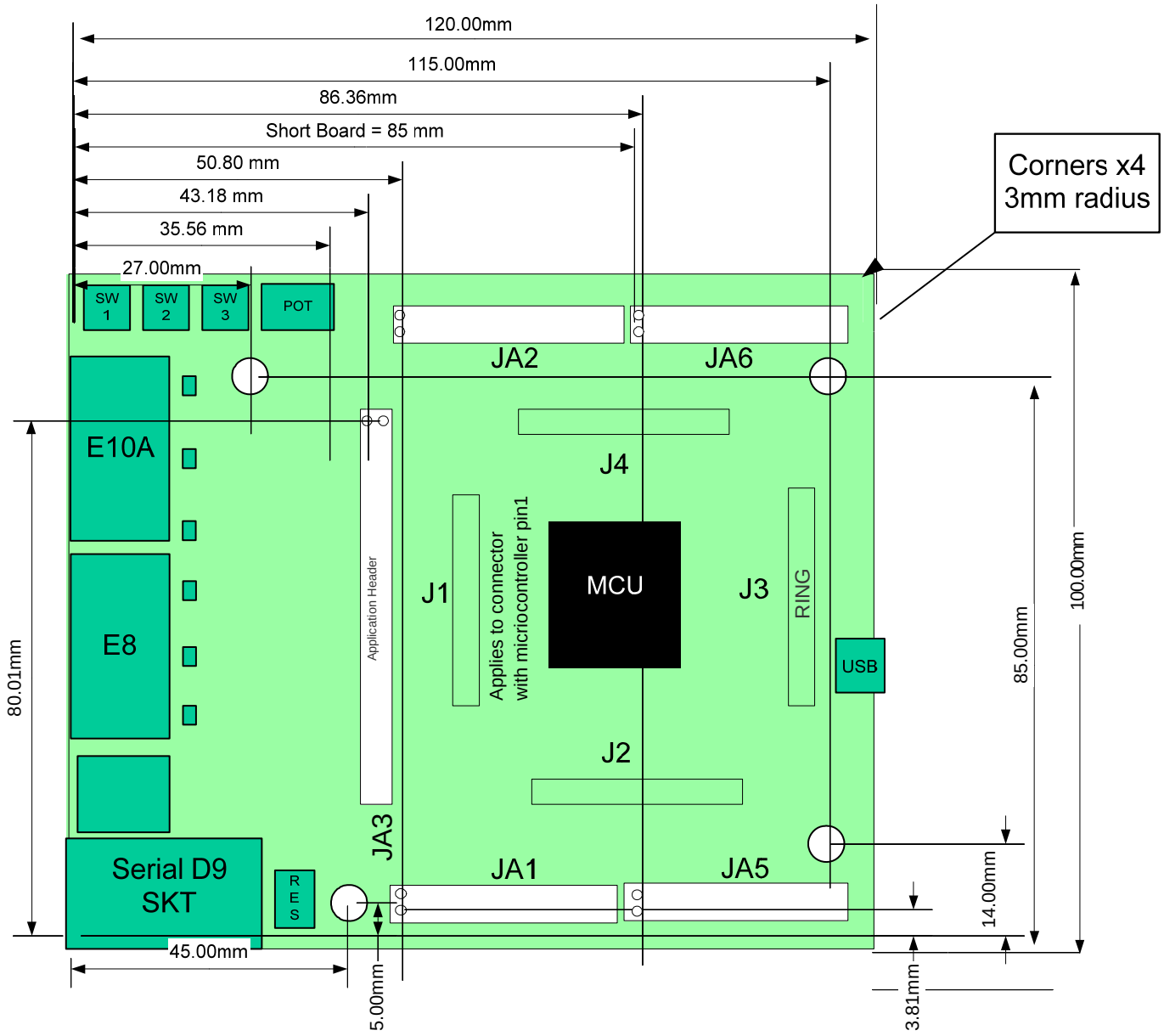



Figure 4-2: Board Dimensions

# Chapter 5. Block Diagram

Figure 5-1 shows the CPU board components and their connectivity.

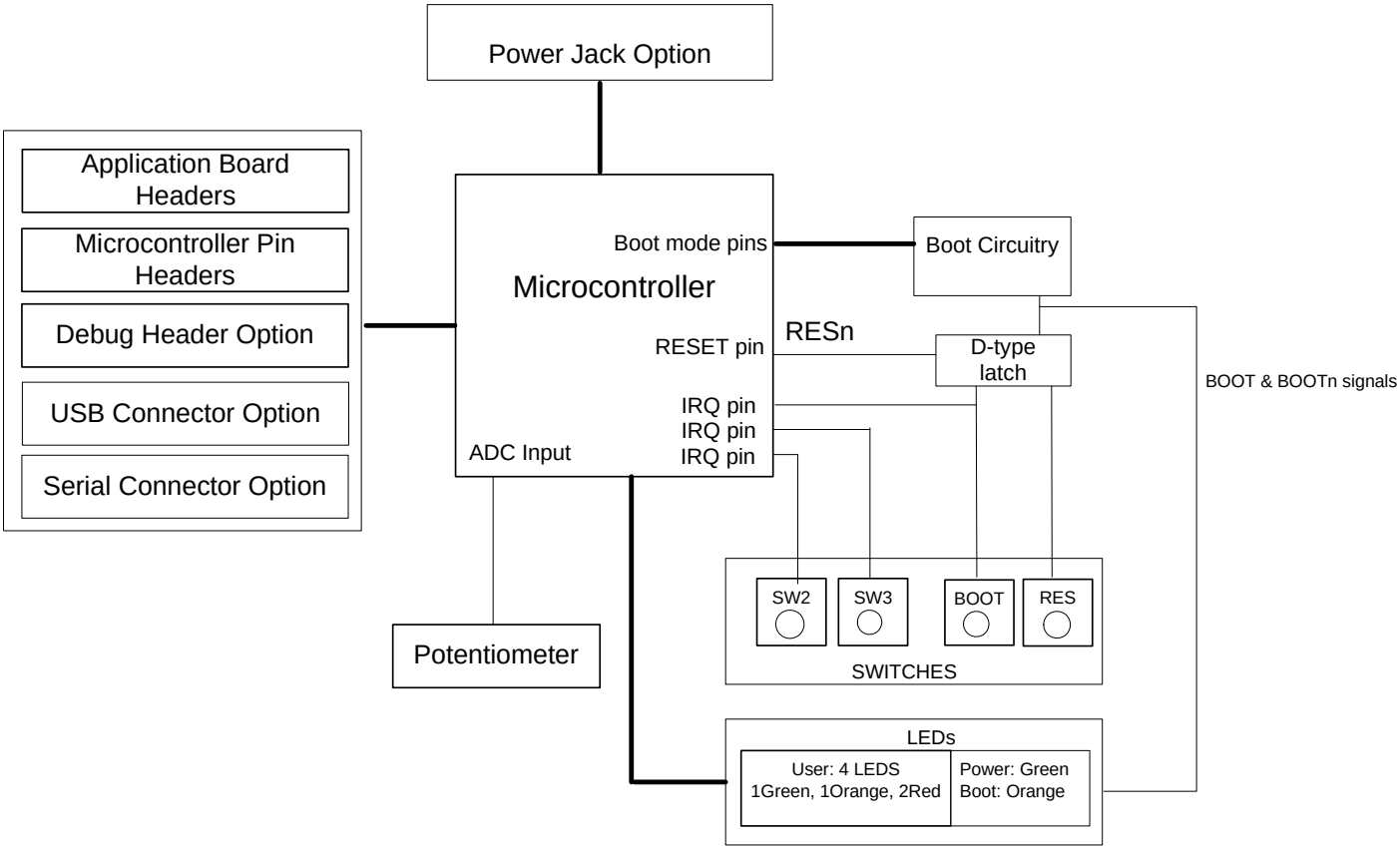



Figure 5-1: Block Diagram

Figure 5-2 shows the connections to the RSK.

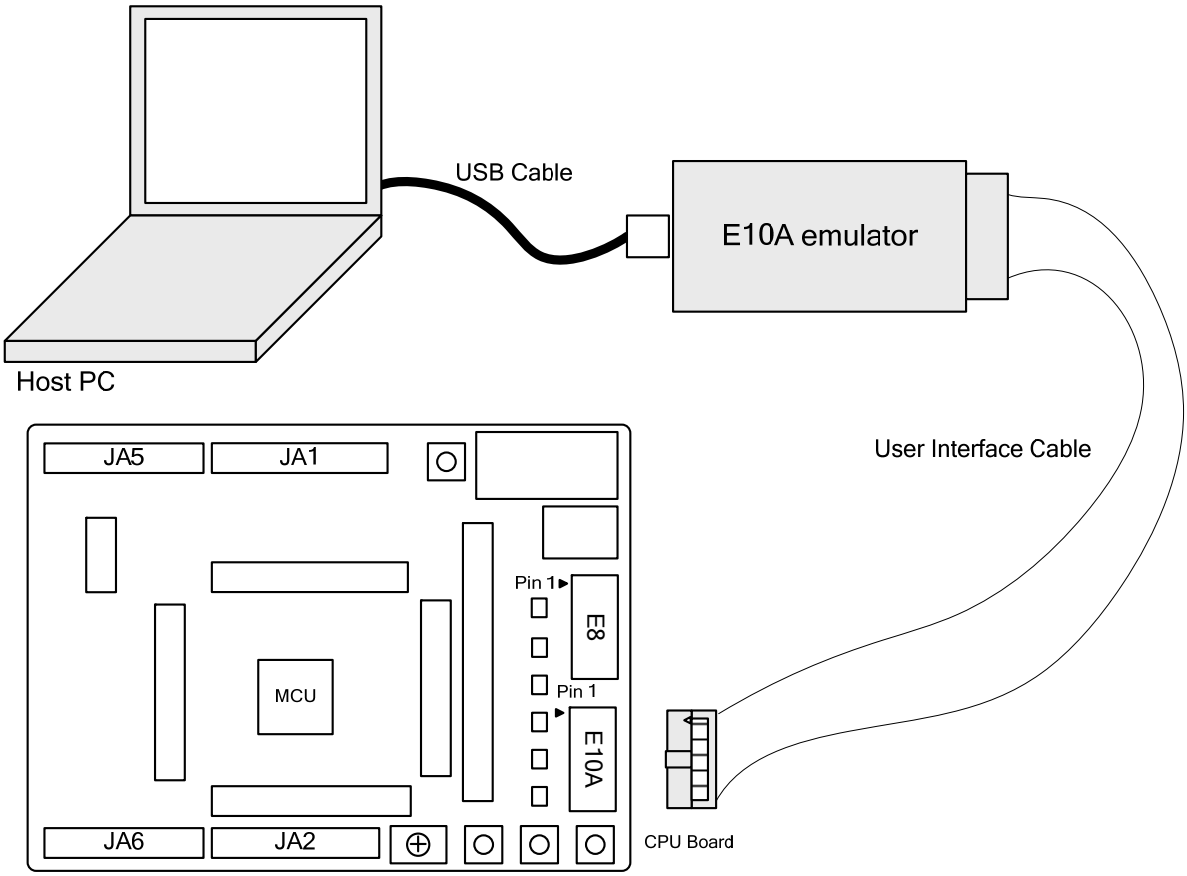



Figure 5-2: RSK Connections

# Chapter 6. User Circuitry

## 6.1. Switches

There are four switches located on the CPU board. The function of each switch and its connection are shown in Table 6-1.

| Switch | Function | Microcontroller |
|---|---|---|
| RES | When pressed, the RSK microcontroller is reset. | RESn, Pin 91 |
| SW1/BOOT* | Connects to an IRQ input for user controls.<br>The switch is also used in conjunction with the RES switch to place the device in BOOT mode when not using the E10A debugger. | IRQ0n, Pin 84<br>(Port 1 pin 0) |
| SW2* | Connects to an IRQ line for user controls. | IRQ1n, Pin 85<br>(Port 1, pin 1) |
| SW3* | Connects to the ADC trigger input. Option link allows connection to IRQ line. The option is a pair of 0R links. For more details on option links, please refer to Sec 6.6. | IRQ3n_ADTRGn, Pin 87<br>(Port 1, pin 3) |

Table 6-1: Switch Functions

*Refer to schematic for detailed connectivity information.

## 6.2. LEDs

There are six LEDs on the RSK board. The green 'POWER' LED lights when the board is powered. The orange BOOT LED indicates the device is in BOOT mode when lit. The four user LEDs are connected to an IO port and will light when their corresponding port pin is set low.

Table 6-2, below, shows the LED pin references and their corresponding microcontroller port pin connections.

| LED Reference (As shown on silkscreen) | Colour | Microcontroller Port Pin function | Microcontroller Pin Number |
|---|---|---|---|
| LED0 | Green | Port B.3 | 3 |
| LED1 | Orange | Port C.2 | 116 |
| LED2 | Red | Port C.3 | 117 |
| LED3 | Red | Port 1.2 | 86 |

Table 6-2: LED Port

## 6.3. Potentiometer

A single turn potentiometer is connected to channel AN0 (P5.0, pin 118) of the microcontroller. This may be used to vary the input analog voltage value to this pin between AVCC and Ground.

## 6.4. Serial port

Serial port SCI0 is connected to the standard RS232 header. Serial port SCI5 can optionally be connected to the RS232 header. The connections to be fitted are listed in the Table 6-3.

| Description | Function | Circuit Net Name | CPU's Pin | Fit for RS232 | Remove for RS232 |
|---|---|---|---|---|---|
| SCI0 | Default serial port | TXD0 | 52 | R31 | R37 |
| SCI0 | Default serial port | RXD0 | 51 | R30 | R36 |
| SCI5 | Spare Serial Port | TXD5 | 93 | R34, R15 | - |
| SCI5 | Spare Serial Port | RXD5 | 94 | R35, R28 | - |

Table 6-3: Serial Port settings

The SCI0 port is also available on J2 and JA2 (R59 and R70 must be fitted) headers. The SCI5 port is available on J3 and JA6 headers..

## 6.5. Debug LCD Module

A debug LCD module is supplied to be connected to the connector marked 'LCD', so that the debug LCD module lies over J2. Care should be taken to ensure the pins are inserted correctly into LCD. The debug LCD module uses a 4 bit interface to reduce the pin allocation. No contrast control is provided; this is set by a resistor on the supplied display module. The module supplied with the RSK only supports 5V operation.

Table 6-4 shows the pin allocation and signal names used on this connector.

| LCD | | | | | |
|---|---|---|---|---|---|
| Pin | Circuit Net Name | Device Pin | Pin | Circuit Net Name | Device Pin |
| 1 | Ground | - | 2 | 5V Only | - |
| 3 | No Connection | - | 4 | DLCDRS (PA0) | 134 |
| 5 | R/W (Wired to Write only) | - | 6 | DLCDE + 100k pull down to ground (PA2) | 136 |
| 7 | No Connection | - | 8 | No connection | - |
| 9 | No Connection | - | 10 | No connection | - |
| 11 | DLCDD4 (PB4) | 130 | 12 | DLCDD5 (PB5) | 131 |
| 13 | DLCDD6 (PB6) | 132 | 14 | DLCDD7 (PB7) | 5 |

Table 6-4 Debug LCD Module Connections

## 6.6.Option Links

Table 6-5 below describes the function of the option links contained on this RSK board and associated with Serial Port Configuration. The default configuration is indicated by BOLD text.

| Option Link Settings | | | | |
|---|---|---|---|---|
| Reference | Function | Fitted | Alternative (Removed) | Related To |
| R15 | Serial Port Configuration | Connects serial port SCI5 (Tx) to D-type connector (J8). | **Disconnects serial port SCI5 (Tx) from D-type connector (J8).** | R28, R34, R35 |
| R19 | Serial Port configuration | Disables RS232 Serial Transceiver | **Enables RS232 Serial Transceiver** | - |
| R28 | Serial Port Configuration | Connects serial port SCI5 (Rx) to D-type connector (J8). | **Disconnects serial port SCI5 (Rx) from D-type connector (J8).** | R15, R34, R35 |
| R30 | Serial Port Configuration | **Routes on-board serial port to SCI0 (Rx) microcontroller pin.** | Disconnects on-board serial port from the CPU's SCI0 (Rx) pin. | R31, R32, R33, R36, R37 |
| R31 | Serial Port Configuration | **Routes on-board serial port to SCI0 (Tx) microcontroller pin.** | Disconnects on-board serial port from the CPU's SCI0 (Tx) pin. | R30, R32, R33, R36, R37 |
| R32 | Serial Port Configuration | Routes serial port SCI0 (Tx) to JA6 header. | **Disconnects serial port SCI0 (Tx) from JA6 header.** | R30, R31, R33 |
| R33 | Serial Port Configuration | Routes serial port SCI0 (Rx) to JA6 header. | **Disconnects serial port SCI0 (Rx) from JA6 header.** | R30, R31, R32 |
| R34 | Serial Port Configuration | Routes on-board serial port to SCI5 (Tx) microcontroller pin. | **Disconnects on-board serial port from SCI5 (Tx) CPU pin.** | R15, R28, R35 |
| R35 | Serial Port Configuration | Routes on-board serial port to SCI5 (Rx) microcontroller pin. | **Disconnects on-board serial port from SCI5 (Rx) CPU pin.** | R15, R28, R34 |
| R36 | Serial Port Configuration | Connects PTRX of programming port to the on-board serial port (J8). | **Disconnects programming port PTRX from the on-board serial port (J8).** | R37, R31, R30 |
| R37 | Serial Port Configuration | Connects PTTX of programming port to the on-board serial port (J8). | **Disconnects programming port PTTX from the on-board serial port (J8).** | R36, R30. R31 |

Table 6-5: **Serial port configuration links.**

**Table 6-6** below describes the function of the option links associated with application board interface. The default configuration is indicated by **BOLD** text.

| Option Link Settings | | | | |
|---|---|---|---|---|
| Reference | Function | Fitted | Alternative (Removed) | Related To |
| R68 | Application board interface | **Use DA0 of application board interface.** | Use AN6 of application board interface. | R108 |
| R108 | Application board interface | Use AN6 of application board interface. | **Use DA0 of application board interface.** | R68 |

| Option Link Settings | | | | |
|---|---|---|---|---|
| Reference | Function | Fitted | Alternative (Removed) | Related To |
| R71 | Application board interface | Use DA1 of application board interface. | Use AN7 of application board interface. | R111 |
| R111 | Application board interface | Use AN7 of application board interface. | Use DA1 of application board interface. | R71 |
| R60 | Application board interface | Use AN0 of application board interface. | Use ADPOT of application board interface. | R96 |
| R96 | Application board interface | Use ADPOT of application board interface. | Use AN0 of application board interface. | R60 |
| R95 | Application board interface | Use IRQ3n of application board interface. | Use ADTRG of application board interface. | R56 |
| R56 | Application board interface | Use ADTRGn of application board interface. | Use IRQ3n of application board interface. | R95 |
| R114 | Application board interface | Use TIOCA2 of application board interface. | Use Up of application board interface. | R69 |
| R69 | Application board interface | Use Up of application board interface. | Use TIOCA2 of application board interface. | R114 |
| R116 | Application board interface | Use TIOCB2 of application board interface. | Use Un of application board interface. | R115 |
| R115 | Application board interface | Use Un of application board interface. | Use TIOCB2 of application board interface. | R116 |
| R81 | Application board interface | Use TIOCA0 of application board interface | Use Vp of application board interface | R75 |
| R75 | Application board interface | Use Vp of application board interface | Use TIOCA0 of application board interface | R81 |
| R90 | Application board interface | Use TIOCB0 of application board interface | Use Vn of application board interface | R84 |
| R84 | Application board interface | Use Vn of application board interface | Use TIOCB0 of application board interface | R90 |
| R85 | Application board interface | Use IO5 of application board interface | Use Wp of application board interface | R86 |
| R86 | Application board interface | Use Wp of application board interface | Use IO5 of application board interface | R85 |
| R88 | Application board interface | Use IO4 of application board interface | Use Wn of application board interface | R74 |
| R74 | Application board interface | Use Wn of application board interface | Use IO4 of application board interface | R88 |

| Option Link Settings | | | | |
|---|---|---|---|---|
| Reference | Function | Fitted | Alternative (Removed) | Related To |
| R67 | Application board interface | **Use IO3 of application board interface** | Use UD of application board interface | R78 |
| R78 | Application board interface | Use UD of application board interface | **Use IO3 of application board interface** | R67 |
| R82 | Application board interface | Use IO2 of application user interface | **Use TxD0 for onboard RS232 module** | R70 |
| R70 | Application board interface | **Use TxD0 of for onboard RS232 module** | Use IO2 of application user interface | R82 |
| R76 | Application board interface | Use IO1 of application board interface | **Use RxD0 for onboard RS232 module** | R59 |
| R59 | Application board interface | **Use RxD0 for onboard RS232 module** | Use IO1 of application board interface | R76 |
| R79 | Application board interface | Use IO0 of application board interface | **Use CLK0 for onboard RS232 module** | R66 |
| R66 | Application board interface | **Use CLK0 for onboard RS232 module** | Use IO0 of application board interface | R79 |
| R54 | Application board interface | Use WDTOVF of application board interface | **Use TDO of E10A debugger interface** | R123 |
| R123 | Application board interface | **Use TDO of E10A debugger interface** | Use WDTOVF of application board interface | R54 |

Table 6-6: Application board interface links.

Table 6-7 below describes the function of the option links associated with E8 and E10A debuggers. The default configuration is indicated by **BOLD** text.

| Option Link Settings | | | | |
|---|---|---|---|---|
| Reference | Function | Fitted | Alternative (Removed) | Related To |
| R4 | E8 | **Enables E8** | | |
| R132 | E10A | Enables E10A, also can be enabled by fitting J15. | **E10A is disabled, can be enabled if J15 is set.** | E10A_EN (J15) jumper |

Table 6-7: E8 and E10A debugger links.

Table 6-8 below describes the function of the option links associated with power source. The default configuration is indicated by **BOLD** text.

| Option Link Settings | | | | |
|---|---|---|---|---|
| Reference | Function | Fitted | Alternative (Removed) | Related To |
| R3 | Power source | **Enables external 5V power supply from 'PWR' (J7) connector.** | Disables power supply from 'PWR' (J7) connector. | R13, R47, R48 |
| R13 | USB Power source | Enables USB VBUS as power supply for this RSK board. | Disables USB VBUS as power supply. | R3, R50 |
| R18 | 3V3 power source | Board can be powered from external source CON_3V3. | **Board can't be powered from external source CON_3V3.** | R24, R40, R52 |
| R22 | Power source | **Enables power supply for E8.** | Disables E8 power supply | R3, R13 |
| R24 | Power source | **Enables 3V3 power supply for on-board devices.** | Disables 3V3 power supply for on-board devices. Current can be measured across R24 | R18, R40 |
| R40 | 3V3 power source | **The RSK board uses on-board voltage regulator.** | The board can be powered from CON_3V3 header. | R18, R24 |
| R47 | Power source | **LCD is powered directly from PWR connector or from CON_5V header** | LCD is not powered directly from PWR connector or from CON_5V header | R49, R51 |
| R48 | 5V External power supply | Board can be powered from external source CON_5V | **Board cannot be powered from external source CON_5V.** | R50, R52 |
| R49 | USB Power source | Enables on-board debug LCD power supply from USB VBUS. | **Disables on-board debug LCD power supply from USB VBUS.** | R13, R47, R50, R51 |
| R50 | USB Power source | Enables USB VBUS as 5V power supply for an external application boards. | **Disconnects USB VBUS from external application board header.** | R13 |
| R51 | Power source | **Enables on-board LCD to be powered from external 5V PSU** | Disables on-board LCD to be powered from external PSU | R47, R49 |
| R52 | Power source | **Enables power supply for a general application board from external 5V PSU** | Disables power supply of a general application board from external 5V PSU | R48, R50 |
| R42 | Ground | **Enables ground connection to ADC module.** | Disconnects ground connection to ADC module. | - |

Table 6-8: Power configuration links.

Table 6-9 below describes the function of the option links associated with clock configuration. The default configuration is indicated by BOLD text.

| Option Link Settings | | | | |
|---|---|---|---|---|
| Reference | Function | Fitted | Alternative (Removed) | Related To |
| R93 | 32.768 KHz Clock Oscillator | Routes OSC1 CPU pin to J3 header | **OSC1 CPU pin and J3 header are not connected** | R94, R103, R105 |
| R94 | 32.768 KHz Clock Oscillator | Routes OSC2 CPU pin to J3 header | **OSC2 CPU pin and J3 header are not connected** | R93, R103, R105 |
| R103 | 32.768 KHz Clock Oscillator | **On-board low-speed clock source is used** | External clock source is used | R93, R94, R104 |
| R105 | 32.768 KHz Clock Oscillator | **On-board low-speed clock source is used** | External clock source is used | R94, R93, R103 |
| R98 | 32.768 KHz Clock Oscillator | Parallel resistor for a crystal | **Not fitted** | - |
| R99 | 12 MHz Clock Oscillator | Routes EXTAL CPU pin to J3 header. | **EXTAL CPU pin and J3 header are not connected** | R102, R101, R100 |
| R102 | 12 MHz Clock Oscillator | Routes XTAL CPU pin to J3 and JA2 headers | **XTAL CPU pin and J3 and JA2 headers are not connected** | R99, R101, R100 |
| R101 | 12 MHz Clock Oscillator | **On-board main clock source is used** | External clock source is used | R99, R102 |
| R100 | 12 MHz Clock Oscillator | Parallel resistor for a crystal | **Not fitted** | - |

Table 6-9: Clock configuration links.

Table 6-10 below describes the function of the option links associated with reference voltage source. The default configuration is indicated by **BOLD** text.

| Option Link Settings | | | | |
|---|---|---|---|---|
| Reference | Function | Fitted | Alternative (Removed) | Related To |
| R64 | Voltage Reference Source | **Voltage Reference set to Board_ Vcc signal.** | Voltage Reference taken from external connector. | R83 |
| R83 | Voltage Reference Source | Voltage Reference is taken from external connector. | **Voltage Reference set to Board_Vcc signal.** | R64 |

Table 6-10: Voltage reference links.

Table 6-11 below describes the function of the option links associated with analog power supply. The default configuration is indicated by **BOLD** text.

| Option Link Settings | | | | |
|---|---|---|---|---|
| Reference | Function | Fitted | Alternative (Removed) | Related To |
| R21 | Analog Voltage Source | **Analog Voltage Source is set to on-board Vcc.** | Analog Voltage Source is taken from external connector. | R46 |
| R46 | Analog Voltage Source | Analog Voltage Source is taken from external connector. | **Analog voltage source is set to on-board Vcc.** | R21 |
| R137 | Analog Voltage Ground | Analog Voltage Ground is routed to external connector. | **Analog Voltage Ground is disconnected from external connector.** | - |

Table 6-11: Analog power supply links.

Table 6-12 below describes the function of the option links associated with MCU modes. The default configuration is indicated by BOLD text.

| Option Link Settings | | | | |
|---|---|---|---|---|
| Reference | Function | Fitted | Alternative (Removed) | Related To |
| R44 | MCU Mode, USB unit | The CPU is self powered. | **The CPU is power from USB bus.** | J10 |
| R131 | MCU Mode | Enables SDRAM interface. | **Disables SDRAM interface.** | J14 |
| R130 | MCU Mode, USB unit | USB dedicated clock is EXTAL × 3 (choose this option if 16 MHz crystal is used). | **USB dedicated clock is EXTAL × 4 (choose this option if 12 MHz crystal is used).** | J13 |
| R133 | MCU Boot mode | Serial Boot Mode is selected. | **USB Boot Mode is selected.** | J16 |

Table 6-12: MCU mode links.

## 6.7. Oscillator Sources

Two crystal oscillators are fitted on the RSK and used to supply the main clock input to the Renesas microcontroller. Table 6-13 details the oscillators that are fitted and alternative footprints provided on this RSK:

| Component | | |
|---|---|---|
| Crystal (X1) | Fitted | 12.0 MHz (HC49/4H package) |
| Crystal (X2) | Fitted | 32.768 KHz |

Table 6-13: Oscillators / Resonators

## 6.8. Reset Circuit

The CPU Board includes a simple latch circuit that links the mode selection and reset circuit. This provides an easy method for swapping the device between Boot Mode and User mode. This circuit is not required on customer's boards as it is intended for providing easy evaluation of the operating modes of the device on the RSK. Please refer to the hardware manual for more information on the requirements of the reset circuit.

The Reset circuit operates by latching the state of the boot switch on pressing the reset button. This control is subsequently used to modify the mode pin states as required.

The mode pins should change state only while the reset signal is active to avoid possible device damage.

The reset is held in the active state for a fixed period by a pair of resistors and a capacitor. Please check the reset requirements carefully to ensure the reset circuit on the user's board meets all the reset timing requirements.

## 6.9. USB port

This RSK has a Full-speed (12 Mbps) USB port compliant to USB 2.0 specification. It is available as J12 on the RSK. This port allows Boot mode programming using USB Direct connection. For more details please refer to *H8SX/1668R Group Hardware Manual.*

# Chapter 7. Modes

This RSK supports two Boot modes and Single Chip mode.

Details of programming the FLASH memory is described in the H8SX/1668R Group Hardware Manual.

## 7.1. Boot mode

The boot mode settings for this RSK are shown in Table 7-1: Boot Mode pin settings below:

| EMLE | MD2 | MD1 | MD0 | PM2 | LSI State after Reset End |
|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 0 | SCI boot mode |
| 0 | 0 | 1 | 0 | 1 | USB boot mode |

Table 7-1: Boot Mode pin settings

The software supplied with this RSK supports debugging with E10A which does not need Boot mode. To enter the Boot mode manually, do not connect the E10A in this case. Press and hold the SW1/BOOT. The BOOT LED will be illuminated to indicate that the microcontroller is in boot mode.

SCI boot mode: boot mode executes programming/erasure of the user MAT or user boot MAT by means of the control command and program data transmitted from the externally connected host via the on-chip SCI_4.

USB boot mode: executes programming/erasing of the user MAT by means of the control command and program data transmitted from the externally connected host via the USB.

## 7.2. Singe chip mode

This is default operating mode of this RSK. Refer to H8SX/1668R Group Hardware Manual for details of Single chip mode. The Single chip mode settings for this RSK are shown in Table 7-2: Single chip mode pin settings below:

| EMLE | MD2 | MD1 | MD0 | LSI State after Reset End |
|---|---|---|---|---|
| 0 | 1 | 1 | 1 | Single chip Mode |

Table 7-2: Single chip Mode pin settings

Programming/erasure of the user MAT is executed by downloading an on-chip program. The user boot MAT cannot be programmed/erased in user program mode.

# Chapter 8. Programming Methods

The board is intended for use with HEW and the supplied E10A debugger. Refer to H8SX/1668R Group Hardware Manual for details of programming the microcontroller without using these tools. Please note that to use E10A debugger, jumper E10A_EN (J15) must be fitted.

# Chapter 9. Headers

## 9.1. Microcontroller Headers

Table 9-1 to Table 9-4 show the microcontroller pin headers and their corresponding microcontroller connections. The header pins connect directly to the microcontroller pin unless otherwise stated.

| J1 | | | | | |
|---|---|---|---|---|---|
| Pin | Circuit Net Name | Device Pin | Pin | Circuit Net Name | Device Pin |
| 1 | CS1n | 1 | 2 | CS2n | 2 |
| 3 | LED0 | 3 | 4 | GROUND | 4 |
| 5 | DLCDD7 | 5 | 6 | UC_VCC | 6 |
| 7 | MD2 | 7 | 8 | TxD6 | 8 |
| 9 | RxD6 | 9 | 10 | PM2 | 10 |
| 11 | A23 | 11 | 12 | A22 | 12 |
| 13 | A21 | 13 | 14 | A20 | 14 |
| 15 | A19 | 15 | 16 | GROUND | 16 |
| 17 | A18 | 17 | 18 | A17 | 18 |
| 19 | A16 | 19 | 20 | A15 | 20 |
| 21 | A14 | 21 | 22 | A13 | 22 |
| 23 | GROUND | 23 | 24 | A12 | 24 |
| 25 | UC_VCC | - | 26 | A11 | 26 |
| 27 | A10 | 27 | 28 | A9 | 28 |
| 29 | A8 | 29 | 30 | A7 | 30 |
| 31 | A6 | 31 | 32 | GROUND | 32 |
| 33 | A5 | 33 | 34 | A4 | 34 |
| 35 | A3 | 35 | 36 | A2 | 36 |

Table 9-1: J1

| J2 | | | | | |
|---|---|---|---|---|---|
| Pin | Circuit Net Name | Device Pin | Pin | Circuit Net Name | Device Pin |
| 1 | A1 | 37 | 2 | A0 | 38 |
| 3 | EMLE | 39 | 4 | PM3 | 40 |
| 5 | PM4 | 41 | 6 | UC_VCC | - |
| 7 | NC | - | 8 | NC | - |
| 9 | GROUND | - | 10 | VBUS_DET | 46 |
| 11 | MD_CLK | 47 | 12 | GROUND | 48 |
| 13 | IO0_CLK0 | 49 | 14 | UC_VCC | 50 |
| 15 | IO1_RxD0 | 51 | 16 | IO2_TxD0 | 52 |
| 17 | IO3_UD | 53 | 18 | IO4_Wn | 54 |
| 19 | IO5_Wp | 55 | 20 | TIOCA0_Vp | 56 |
| 21 | TIOCB0_Vn | 57 | 22 | TRISTn | 109 |
| 23 | IO6 | 59 | 24 | IO7 | 60 |
| 25 | NMIn | 61 | 26 | DREQ1n | 62 |
| 27 | TEND1n | 63 | 28 | UC_VCC | 64 |
| 29 | D0 | 65 | 30 | D1 | 66 |
| 31 | D2 | 67 | 32 | D3 | 68 |
| 33 | GROUND | 69 | 34 | D4 | 70 |
| 35 | D5 | 71 | 36 | D6 | 72 |

Table 9-2: J2

| J3 | | | | | |
|---|---|---|---|---|---|
| Pin | Circuit Net Name | Device Pin | Pin | Circuit Net Name | Device Pin |
| 1 | D7 | 73 | 2 | UC_VCC | 74 |
| 3 | D8 | 75 | 4 | D9 | 76 |
| 5 | D10 | 77 | 6 | D11 | 78 |
| 7 | GROUND | 79 | 8 | D12 | 80 |
| 9 | D13 | 81 | 10 | D14 | 82 |
| 11 | D15 | 83 | 12 | IRQ0n | 84 |
| 13 | IRQ1n | 85 | 14 | LED3 | 86 |
| 15 | IRQ3n_ADTRGn | 87 | 16 | GROUND | 88 |
| 17 | CON_OSC2 (*) | 89 | 18 | CON_OSC1 (*) | 90 |
| 19 | RESn | 91 | 20 | NC | - |
| 21 | TxD5 | 93 | 22 | RxD5 | 94 |
| 23 | WDTOVFn_TDO | 95 | 24 | GROUND | 96 |
| 25 | CON_XTAL (*) | 97 | 26 | CON_EXTAL (*) | 98 |
| 27 | UC_VCC | 99 | 28 | P1_6 | 100 |
| 29 | P1_7 | 101 | 30 | STBYn | 102 |
| 31 | GROUND | - | 32 | DACK1n | 104 |
| 33 | TIOCA2_Up | 105 | 34 | TIOCB2_Un | 106 |
| 35 | PTTX | 107 | 36 | PTRX | 108 |

Table 9-3: J3

| J4 | | | | | |
|---|---|---|---|---|---|
| Pin | Circuit Net Name | Device Pin | Pin | Circuit Net Name | Device Pin |
| 1 | TRSTn | 109 | 2 | UC_VCC | - |
| 3 | TMS | 111 | 4 | GROUND | - |
| 5 | TDI | 113 | 6 | TCK | 114 |
| 7 | MD0 | 115 | 8 | LED1 | 116 |
| 9 | LED2 | 117 | 10 | ADPOT_AN0 | 118 |
| 11 | AN1 | 119 | 12 | AN2 | 120 |
| 13 | CON_AVCC | 121 | 14 | AN3 | 122 |
| 15 | AVSS | 123 | 16 | AN4 | 124 |
| 17 | CON_VREF | 125 | 18 | AN5 | 126 |
| 19 | DA0_AN6 | 127 | 20 | DA1_AN7 | 128 |
| 21 | MD1 | 129 | 22 | DLCDD4 | 130 |
| 23 | DLCDD5 | 131 | 24 | DLCDD6 | 132 |
| 25 | MD3 | 133 | 26 | DLCDRS | 134 |
| 27 | WRn | 135 | 28 | DLCDE | 136 |
| 29 | LLWRn | 137 | 30 | LHWRn | 138 |
| 31 | RDn | 139 | 32 | ASn | 140 |
| 33 | GROUND | 141 | 34 | BCLK | 142 |
| 35 | UC_VCC | 143 | 36 | CS0n | 144 |

Table 9-4: J4

## 9.2. Application Headers

Table 9-5 to Table 9-9 below show the standard application header connections.

| JA1 | | | | | | | |
|---|---|---|---|---|---|---|---|
| Pin | Generic Header Name | CPU board Signal Name | Device Pin | Pin | Generic Header Name | CPU board Signal Name | Device Pin |
| 1 | 5V | CON_5V | - | 2 | 0V | GROUND | - |
| 3 | 3V3 | CON_3V3 | - | 4 | 0V | GROUND | - |
| 5 | AVCC | CON_AVCC | 121 | 6 | AVss | CON_AVSS | 123 |
| 7 | AVref | CON_VREF | 125 | 8 | ADTRG | ADTRGn | 87 |
| 9 | AD0 | AN0 (**) | 118 | 10 | AD1 | AN1 | 119 |
| 11 | AD2 | AN2 | 120 | 12 | AD3 | AN3 | 122 |
| 13 | DAC0 | DA0 (**) | 127 | 14 | DAC1 | DA1 | 128 |
| 15 | IO_0 | IO0 (**) | 49 | 16 | IO_1 | IO1 (**) | 51 |
| 17 | IO_2 | IO2 (**) | 52 | 18 | IO_3 | IO3 (**) | 53 |
| 19 | IO_4 | IO4 (**) | 54 | 20 | IO_5 | IO5 (**) | 55 |
| 21 | IO_6 | IO6 | 59 | 22 | IO_7 | IO7 | 60 |
| 23 | IRQ3 | IRQ3n (**) | 87 | 24 | IIC_EX | NC | - |
| 25 | IIC_SDA | SDA0 | - | 26 | IIC_SCL | SCL0 | - |

Table 9-5: JA1 Standard Generic Header

| JA2 | | | | | | | |
|---|---|---|---|---|---|---|---|
| Pin | Generic Header Name | CPU board Signal Name | Device Pin | Pin | Generic Header Name | CPU board Signal Name | Device Pin |
| 1 | RESn | RESn | 91 | 2 | EXTAL | CON_EXTAL | 97 |
| 3 | NMIn | NMIn | 61 | 4 | VSS1 | GROUND | - |
| 5 | WDT_OVF | WDTOVF | 95 | 6 | SCIaTX | TxD0 (**) | 52 |
| 7 | IRQ0 | IRQ0n | 84 | 8 | SCIaRX | RxD0 (**) | 51 |
| 9 | IRQ1 | IRQ1n | 85 | 10 | SCIaCK | CLK0 (**) | 49 |
| 11 | UD | UD (**) | 53 | 12 | CTSRTS | NC | - |
| 13 | Up | Up (**) | 105 | 14 | Un | Un (**) | 106 |
| 15 | Vp | Vp (**) | 56 | 16 | Vn | Vn (**) | 57 |
| 17 | Wp | Wp (**) | 55 | 18 | Wn | Wn (**) | 54 |
| 19 | TMR0 | TIOCA0 (**) | 56 | 20 | TMR1 | TIOCA2 (**) | 105 |
| 21 | TRIGa | TIOCB0 | 57 | 22 | TRIGb | TIOCB2 (**) | 106 |
| 23 | IRQ2 | IRQ3n (**) | 87 | 24 | TRISTn | TRISTn | 109 |
| 25 | - | - | - | 26 | - | - | - |

Table 9-6: JA2 Standard Generic Header

| JA5 | | | | | | | |
|---|---|---|---|---|---|---|---|
| Pin | Generic Header Name | CPU board Signal Name | Device Pin | Pin | Generic Header Name | CPU board Signal Name | Device Pin |
| 1 | AD4 | AN4 | 124 | 2 | AD5 | AN5 | 126 |
| 3 | AD6 | AN6 (**) | 127 | 4 | AD7 | AN7 (**) | 128 |
| 5 | CAN1TX | - | - | 6 | CAN1RX | - | - |
| 7 | CAN2TX | - | - | 8 | CAN2RX | - | - |
| 9 | - | - | - | 10 | - | - | - |
| 11 | - | - | - | 12 | - | - | - |
| 13 | - | - | - | 14 | - | - | - |
| 15 | - | - | - | 16 | - | - | - |
| 17 | - | - | - | 18 | - | - | - |
| 19 | - | - | - | 20 | - | - | - |
| 21 | - | - | - | 22 | - | - | - |
| 23 | - | - | - | 24 | - | - | - |

Table 9-7: JA5 Standard Generic Header

| JA6 | | | | | | | |
|---|---|---|---|---|---|---|---|
| Pin | Generic Header Name | CPU board Signal Name | Device Pin | Pin | Generic Header Name | CPU board Signal Name | Device Pin |
| 1 | DREQ | DREQ1n | 62 | 2 | DACK | DACK1n | 104 |
| 3 | TEND | TEND1n | 63 | 4 | STBYn | NC | - |
| 5 | RS232TX | RS232TX | - | 6 | RS232RX | RS232RX | - |
| 7 | SCIbRX | RxD5 | 94 | 8 | SCIbTX | TxD5 | 8 |
| 9 | SCIcTX | TxD6 | 93 | 10 | SCIbCK | | - |
| 11 | SCIcCK | NC | - | 12 | SCIcRX | RxD6 | 9 |
| 13 | - | - | - | 14 | - | - | - |
| 15 | - | - | - | 16 | - | - | - |
| 17 | - | - | - | 18 | - | - | - |
| 19 | - | - | - | 20 | - | - | - |
| 21 | - | - | - | 22 | - | - | - |
| 23 | - | - | - | 24 | - | - | - |

Table 9-8: JA6 Standard Generic Header

| JA3 | | | | | | | |
|---|---|---|---|---|---|---|---|
| Pin | Generic Header Name | CPU board Signal Name | Device Pin | Pin | Generic Header Name | CPU board Signal Name | Device Pin |
| 1 | A0 | A0 | 38 | 2 | A1 | A1 | 37 |
| 3 | A2 | A2 | 36 | 4 | A3 | A3 | 35 |
| 5 | A4 | A4 | 34 | 6 | A5 | A5 | 33 |
| 7 | A6 | A6 | 31 | 8 | A7 | A7 | 30 |
| 9 | A8 | A8 | 29 | 10 | A9 | A9 | 28 |
| 11 | A10 | A10 | 27 | 12 | A11 | A11 | 26 |
| 13 | A12 | A12 | 24 | 14 | A13 | A13 | 22 |
| 15 | A14 | A14 | 21 | 16 | A15 | A15 | 20 |
| 17 | D0 | D0 | 65 | 18 | D1 | D1 | 66 |
| 19 | D2 | D2 | 67 | 20 | D3 | D3 | 68 |
| 21 | D4 | D4 | 70 | 22 | D5 | D5 | 71 |
| 23 | D6 | D6 | 72 | 24 | D7 | D7 | 73 |
| 25 | RDn | RDn | 139 | 26 | WRn | WRn | 135 |
| 27 | CS0n | CS0n | 144 | 28 | CS1n | CS1n | 1 |
| 29 | D8 | D8 | 75 | 30 | D9 | D9 | 76 |
| 31 | D10 | D10 | 77 | 32 | D11 | D11 | 78 |
| 33 | D12 | D12 | 80 | 34 | D13 | D13 | 81 |
| 35 | D14 | D14 | 82 | 36 | D15 | D15 | 83 |
| 37 | A16 | A16 | 19 | 38 | A17 | A17 | 18 |
| 39 | A18 | A18 | 17 | 40 | A19 | A19 | 15 |
| 41 | A20 | A20 | 14 | 42 | A21 | A21 | 13 |
| 43 | A22 | A22 | 12 | 44 | SDCLK | BCLK | 142 |
| 45 | CS2n | CS2n | 2 | 46 | ALE | ASn | 140 |
| 47 | WRHn | LHWRn | 138 | 48 | WRLn | LLWRn | 137 |
| 49 | CASn | - | - | 50 | RASn | - | - |

Table 9-9: JA3 Standard Generic Header

* - Optional link. By default, these signals are disconnected.

** - Optional link. Please refer to schematic for details.

# Chapter 10. Code Development

## 10.1. Overview

Note: For all code debugging using Renesas software tools, the RSK board must be connected to a PC USB port via an E10A. An E10A pod is supplied with the RSK product.

## 10.2. Compiler Restrictions

The compiler supplied with this RSK is fully functional for a period of 60 days from first use. After the first 60 days of use have expired, the compiler will default to a maximum of 64k code and data. To use the compiler with programs greater than this size you need to purchase the full tools from your distributor.

Warning: The protection software for the compiler will detect changes to the system clock. Changes to the system clock back in time may cause the trial period to expire prematurely.

## 10.3. Mode Support

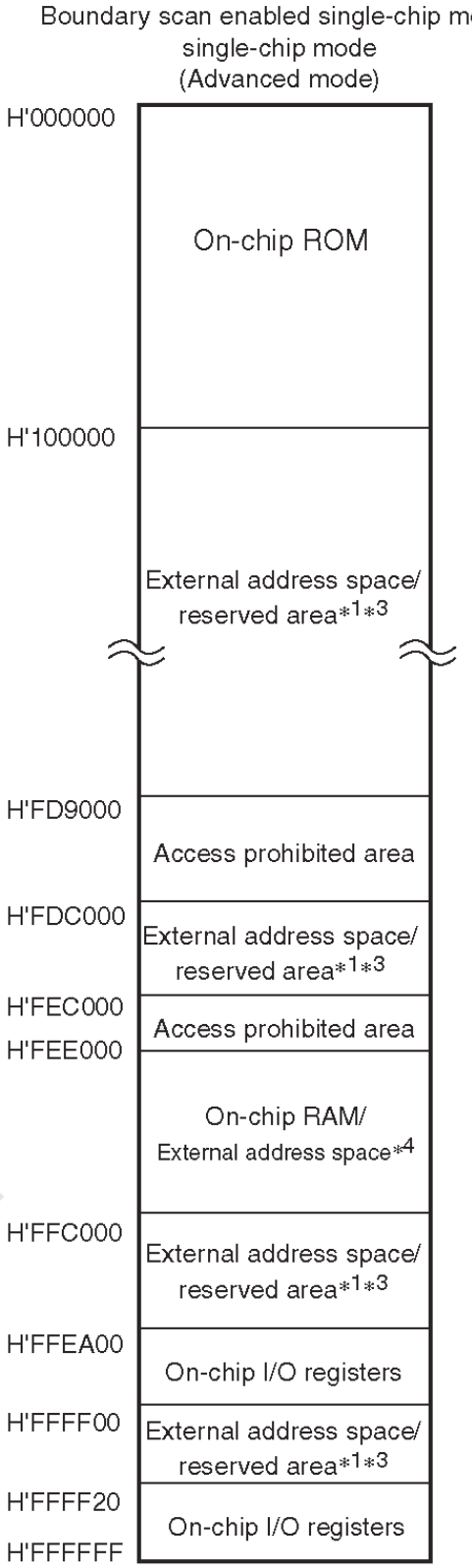
HEW connects to the Microcontroller and programs it via the E10A. Mode support is handled transparently to the user.

## 10.4. Breakpoint Support

HEW supports breakpoints on the user code, both in RAM and ROM.

Double clicking in the breakpoint column in the code sets the breakpoint. Breakpoints will remain unless they are double clicked to remove them.

## 10.5. Memory Map




Notes:1. This area is specified as the external address space when EXPE = 1 and the reserved area when EXPE = 0.
2. The on-chip RAM is used for flash memory programming. Do not clear the RAME bit in SYSCR to 0.
3. Do not access the reserved areas.
4. This area is specified as the external address space by clearing the RAME bit in SYSCR to 0.

Figure 10-1: Memory Map

# Chapter 11. Component Placement

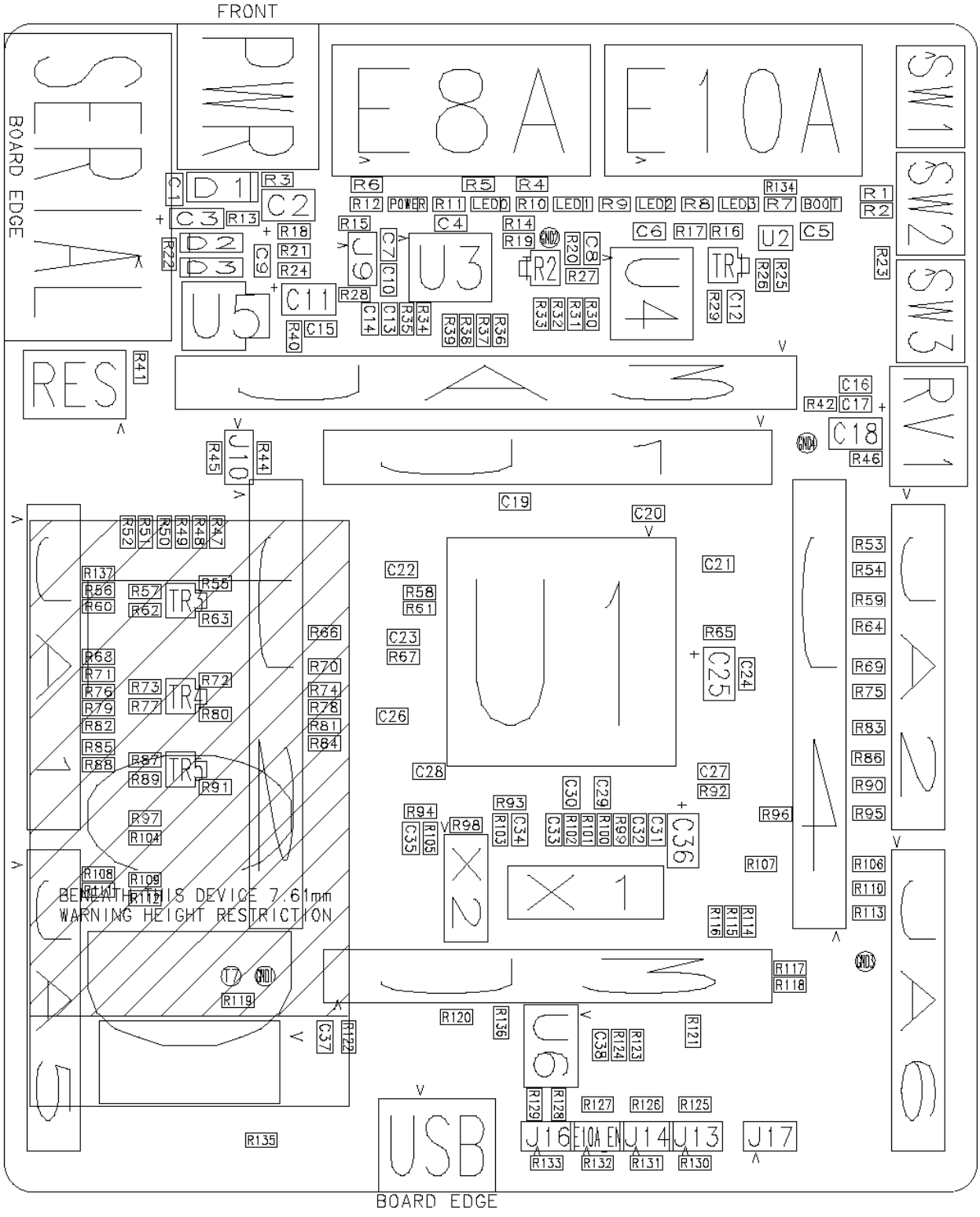



Figure 11-1: Component Placement – Front view

# Chapter 12. Additional Information

For details on how to use High-performance Embedded Workshop (HEW, refer to the HEW manual available on the CD or from the web site.

For information about the H8SX/1668R series microcontrollers refer to the H8SX/1668R Group hardware manual.

For information about the H8SX/1668R assembly language, refer to the H8SX Series Software Manual.

Online technical support and information is available at: http://www.renesas.com/renesas_starter_kits

Technical Contact Details

America: techsupport.rta@renesas.com

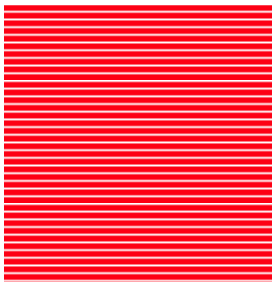
Europe: tools.support.eu@renesas.com

Japan: csc@renesas.com

General information on Renesas Microcontrollers can be found on the Renesas website at: http://www.renesas.com/

Renesas Starter Kit for H8SX/1668R
User's Manual
Publication Date Rev.1.00 04.04.2008
Published by: Renesas Technology Europe Ltd.
Duke’s Meadow, Millboard Road, Bourne End
Buckinghamshire SL8 5FH, United Kingdom

# Renesas Starter Kit for H8SX/1668R
# User's Manual



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